A

Please type a plus sign (+) inside this box → [+]

PTO/SB/05 (4/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	MI22-1284
First Inventor or Application Identifier	Eugene P. Marsh
Title	See 1 in Addendum
Express Mail Label No.	EL 169866407

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)*
   (Submit an original and a duplicate for fee processing)
2. [X] Specification [Total Pages 28]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 2]
4. Oath or Declaration [Total Pages 2]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 C.F.R. § 1.63(d))
   (for continuation/divisional with Box 16 completed)
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
14. [ ] Certified Copy of Priority Document(s)
    (if foreign priority is claimed)
15. [X] Other: See 2 in Addendum

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[X] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: 09/281,735

Prior application information: Examiner H. Vu Group / Art Unit: 2811

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[X] *Customer Number or Bar Code Label* 021567 *(Insert Customer No. or Attach bar code label here)* or [ ] *Correspondence address below*

Name					
Address					
City		State		Zip Code	
Country		Telephone		Fax	

Name (Print/Type)	David G. Latwesen, Ph.D.	Registration No. (Attorney/Agent)	38,533
Signature		Date	10/19/99

Burden Hour Statement. This form is estimated to take 0 2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/281,735
Priority Filing Date ..... March 30, 1999
Inventor ..... Eugene P. Marsh
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2811
Priority Examiner ..... H. Vu
Attorney's Docket No. MI22-1284
Title: Circuitry Comprising Roughened Platinum Layers, Platinum-Containing Materials, Capacitors Comprising Roughened Platinum Layers, Methods of Forming Roughened Layers of Platinum, and Methods of Forming Capacitors

PRELIMINARY AMENDMENT

To: Assistant Commissioner for Patents
Washington, D.C. 20231

From: David G. Latwesen (Tel. 509-624-4276; Fax 509-838-3424)
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

AMENDMENTS

In the Specification

At p. 1, before the "Technical Field" section, insert

--**RELATED PATENT DATA**

This patent resulted from a continuation application of U.S. Patent Application Serial No. 09/281,735, which was filed on March 30, 1999, which is a divisional application of U.S. Patent Application Serial No. 09/141,840, which was filed on August 27, 1998.--.

In the Claims

Cancel claims 1-56.

New Claims

57. An integrated circuit comprising hemispherical grain platinum.

58. An integrated circuit comprising:

a monocrystalline silicon substrate; and

a roughened platinum layer over the substrate, the roughened platinum layer being continuous over an area of the substrate that comprises at least about 4 x 10^6 square Angstroms and comprising pedestals that are at least about 300Å tall within the area.

59. The circuit of claim 58 wherein the platinum layer comprises hemispherical grain platinum.

60. The circuit of claim 58 wherein the area of the substrate comprises a square.

61. An integrated circuit comprising:

a monocrystalline silicon substrate; and

a roughened platinum layer over the substrate, the roughened platinum layer having a continuous surface characterized by columnar pedestals having heights greater than or equal to about one-third of a total thickness of the platinum layer.

62. The circuit of claim 61 wherein the platinum layer has a thickness of at least about 600Å.

63. The circuit of claim 61 wherein the platinum layer has a thickness of greater than or equal to about 400Å.

64. The circuit of claim 61 wherein the platinum layer has a thickness of greater than or equal to about 100Å.

65. The circuit of claim 61 further comprising an adhesion layer between the platinum layer and the substrate, the adhesion layer comprising at least one of titanium nitride, iridium, rhodium, ruthenium, platinum, palladium, osmium, silver, rhodium/platinum alloy, IrO_2, RuO_2, RhO_2, or OsO_2.

66. The circuit of claim 61 wherein the pedestals terminate in dome-shaped tops.

67. The circuit of claim 61 wherein the pedestals terminate in hemispherical tops.

68. A capacitor comprising:

a first capacitor electrode over a monocrystalline silicon substrate;

a second capacitor electrode;

a dielectric layer between the first and second capacitor electrodes; and

wherein at least one of the first and second capacitor electrodes comprises a roughened platinum layer, the roughened platinum layer having a thickness of from about 400Å to about 1000Å and comprising pedestals that are at least about 300Å tall.

69. The capacitor of claim 68 wherein the roughened platinum layer comprises hemispherical grain platinum.

70. The capacitor of claim 68 wherein the roughened platinum layer is over a surface and is continuous over an area of the surface that is at least about 4×10^6 square Angstroms.

71. The capacitor of claim 70 wherein the area comprises a square.

72. A capacitor comprising:

a first capacitor electrode over a monocrystalline silicon substrate;

a second capacitor electrode;

a dielectric layer between the first and second capacitor electrodes; and

wherein at least one of the first and second capacitor electrodes comprises a roughened platinum layer, the roughened platinum layer having a continuous surface characterized by columnar pedestals having heights greater than or equal to about one-third of a total thickness of the platinum layer.

73. The capacitor of claim 72 wherein both capacitor electrodes comprise platinum, but only one of the capacitor electrodes comprises the roughened platinum layer.

74. The capacitor of claim 72 wherein both capacitor electrodes comprise roughened platinum layers.

75. The circuit of claim 72 wherein the pedestals terminate in dome-shaped tops.

76. The circuit of claim 72 wherein the pedestals terminate in hemispherical tops.

REMARKS

Claims 1-56 are canceled, and new claims 57-76 are added. Claims 57-76 are pending in the application, and Applicant requests examination of such pending claims.

Respectfully submitted,

Dated: 10/19/99

By: _____

David G. Latwesen, Ph.D.
Reg. No.: 38,533

EL05[illegible]32007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

CIRCUITRY COMPRISING ROUGHENED PLATINUM LAYERS, PLATINUM-CONTAINING MATERIALS, CAPACITORS COMPRISING ROUGHENED PLATINUM LAYERS, METHODS OF FORMING ROUGHENED LAYERS OF PLATINUM, AND METHODS OF FORMING CAPACITORS

* * * * *

INVENTOR
Eugene P. Marsh

ATTORNEY'S DOCKET NO. MI22-857

CIRCUITRY COMPRISING ROUGHENED PLATINUM LAYERS, PLATINUM-CONTAINING MATERIALS CAPACITORS COMPRISING ROUGHENED PLATINUM LAYERS, METHODS OF FORMING ROUGHENED LAYERS OF PLATINUM, AND METHODS OF FORMING CAPACITORS

TECHNICAL FIELD

The invention pertains to methods of forming and using platinum-containing materials, and to circuitry incorporating roughened layers of platinum.

BACKGROUND OF THE INVENTION

Platinum is a candidate for utilization as a conductive material in advanced semiconductor processing. Platinum can be utilized in an elemental form, or as an alloy (such as, for example, rhodium/platinum), and can be deposited onto a substrate by, for example, sputter deposition or chemical vapor deposition (CVD) methods. Platinum is typically formed to have a relatively smooth upper surface. Such smooth upper surface can be advantageous in, for example, applications in which circuitry is formed over the platinum layer. Specifically, the relatively smooth surface can provide a substantially planar platform upon which other circuitry is formed. However, there can be advantages to incorporating roughened conductive layers into integrated circuitry in applications where high surface area is desired, as with capacitor

electrodes. Accordingly, it would be desirable to develop methods of forming platinum layers having roughened outer surfaces.

In another aspect of the prior art, platinum-comprising materials are frequently utilized as catalysts in, for example, the petroleum industry, as well as in, for example, automobile exhaust systems. Frequently, an efficiency of a catalyst can be improved by enhancing a surface area of the catalyst. Accordingly, it would be desirable to develop methods of enhancing surface area of platinum-comprising materials.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of forming a roughened layer of platinum. A substrate is provided within a reaction chamber. An oxidizing gas is flowed into the reaction chamber, and a platinum precursor is flowed into the chamber. Platinum is deposited from the platinum precursor over the substrate in the presence of the oxidizing gas. A temperature within the chamber is maintained at from about 0°C to less than 300°C during the depositing.

In another aspect, the invention encompasses a circuit comprising a roughened platinum layer over a substrate. The roughened platinum layer has a continuous surface characterized by columnar pedestals.

In yet another aspect, the invention encompasses a platinum catalyst characterized by a continuous outer surface portion of the platinum having a plurality of columnar pedestals that are at least about 400Å tall. The surface portion covers an area that is at least about 4×10^6 square Angstroms.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic, fragmentary, cross-sectional view of a semiconductive wafer fragment processed according to a method of the present invention.

Fig. 2 is a fragmentary top view of the semiconductor wafer fragment of Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that of Fig. 1.

Fig. 4 is a scanning electron microscope (SEM) micrograph of a platinum film produced by CVD of $MeCpPt(Me)_3$.

Fig. 5 is a SEM micrograph of a platinum film produced by CVD of $MeCpPt(Me)_3$ under different conditions than those utilized for forming the film of Fig. 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

The invention encompasses methods of forming platinum layers having roughened outer surfaces, and methods of incorporating such layers into capacitor constructions. Fig. 1 shows a semiconductor wafer fragment 10 at a preliminary processing step of the present invention. Wafer fragment 10 comprises a substrate 12. Substrate 12 can comprise, for example, a monocrystalline silicon wafer lightly doped with a background p-type dopant. To aid in interpretation of the claims that follow, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited

to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

A diffusion region 14 is formed within substrate 12 and defines a node location to which electrical connection with a storage node of a capacitor is to be made. Diffusion region 14 can be formed by, for example, implanting a conductivity enhancing dopant into substrate 12.

An adhesion layer 16 is formed over substrate 12 and in electrical contact with diffusion region 14, and a platinum-comprising layer 18 is formed over adhesion layer 16. Adhesion layer 16 is provided to enhance adhesion of platinum-comprising layer 18 to substrate 12. In other embodiments (not shown) a platinum-comprising layer can be provided directly onto a silicon surface (either the monocrystalline silicon surface of substrate 12, or an intervening amorphous or polycrystalline surface). Such embodiments are less preferred than the shown embodiment due to difficulties of adequately adhering platinum directly to silicon.

Adhesion layer 16 can comprise, for example, at least one of titanium nitride, iridium, rhodium, ruthenium, platinum, palladium, osmium, silver, rhodium/platinum alloy, IrO_2, RuO_2, RhO_2, or OsO_2.

Adhesion layer 16 can be formed by, for example, chemical vapor deposition, and can be formed to a thickness of, for example, less than 100Å.

Platinum-comprising layer 18 can comprise, for example, elemental platinum, or a platinum alloy, such as rhodium/platinum alloy. Platinum-comprising layer 18 is provided to have a roughened outer surface 20. Such can be accomplished by chemical vapor deposition of platinum-comprising layer 18 under relatively low temperature conditions, and in the presence of an oxidizing atmosphere. For instance, a platinum-comprising layer 18 formed as follows will comprise a roughened outer surface 20.

First, substrate 12 is inserted within a CVD reaction chamber. An oxidizing gas and a platinum precursor are flowed into the reaction chamber. Platinum is deposited from the platinum precursor over substrate 12 in the presence of the oxidizing gas. A temperature within the reaction chamber is maintained at from about 0°C to less than 300°C during the depositing, and a pressure within the reactor is preferably maintained at from about 0.5 Torr to about 20 Torr. Suitable control of the temperature and of a relative flow rate of the oxidizing gas to the platinum precursor causes deposited platinum layer 18 to have a roughened outer surface 20. The platinum precursor is flowed into the reaction chamber in a carrier gas, such as, for example, a gas known to be generally inert to reaction with platinum precursor materials, such

as, for example, helium or argon. The platinum precursor can comprise, for example, at least one of $MeCpPtMe_3$, $CpPtMe_3$, $Pt(acetylacetonate)_2$, $Pt(PF_3)_4$, $Pt(CO)_2Cl_2$, cis-$[PtMe_2(MeNC)_2]$, or platinum hexafluoroacetylacetonate; wherein Cp is a cyclopentadienyl group and Me is a methyl group. The oxidizing gas can comprise, for example, at least one of O_2, N_2O, SO_3, O_3, H_2O_2, or NO_x, wherein x has a value of from 1 to 3. In embodiments wherein platinum layer 18 comprises a platinum/metal alloy, at least one other metal precursor can be flowed into the reaction chamber to deposit the platinum as an alloy of the platinum and the at least one other metal. The at least one other metal precursor can comprise, for example, a precursor of rhodium, iridium, ruthenium, palladium, osmium, and/or silver.

The oxidizing gas can assist in deposition of platinum from the platinum-comprising precursor by oxidizing carbon from the precursor during deposition of the platinum. Also, the oxidizing gas can influence a deposition rate of a platinum-comprising layer. Specifically, a greater rate of flow of the oxidizing gas relative to the flow of the platinum precursor can lead to faster deposition of the platinum-comprising layer. The rate of flow of platinum precursor is influenced by a rate of flow of carrier gas through a liquid organic precursor solution, and by a temperature of the precursor solution. In preferred embodiments of the invention, a carrier gas will be flowed through a liquid organic precursor solution at a rate of from about 2 sccm to about 1000 sccm and more

preferably at less than or equal to about 30 sccm. In such preferred embodiments, the oxidizing gas will be flowed at a flow rate of at least about 50 sccm. The organic precursor will preferably be at a temperature of from about 0°C to about 100°C, and more preferably from about 30°C to about 50°C.

A rate of growth of platinum-comprising layer within the reaction chamber is also influenced by a temperature of the substrate. Specifically, if platinum is deposited under conditions wherein the temperature of the substrate is maintained at from about 220°C to less than 300°C, the platinum will deposit at a rate of about 600Å in about 30 seconds. If a temperature of the substrate is reduced to below about 210°C, a rate of deposition of platinum will decrease considerably. It is preferred that a deposition time for a 600Å thick platinum-comprising layer be less than or equal to about 40 seconds to maintain efficiency of a production process. Accordingly, it is preferred that the temperature of the substrate be maintained at above about 210°C, and preferably at from greater than or equal to about 220°C during deposition of the platinum-comprising layer within the reaction chamber.

It is also found that if a temperature is greater than 300°C and less than about 350°C, a deposited platinum layer will have a smooth outer surface, rather than a desired roughened outer surface. Further, if the temperature of the substrate exceeds about 400°C, a deposited platinum surface will have holes extending to a surface underlying the

platinum surface, rather than being a continuous surface overlying a substrate. Accordingly, it is preferred that the temperature of the substrate be well below 400°C, more preferred that the temperature be below 300°C, and even more preferred that the temperature be less than or equal to about 280°C. In preferred embodiments of the present invention, the temperature of the substrate will be maintained at from about 220°C to about 280°C, whereupon it is found that a platinum layer having a roughened outer surface can be deposited to a thickness of about 600Å in about 30 seconds.

Platinum layer 18 is preferably deposited to a thickness of at least about 400Å to avoid having surface anomalies (such as crevices or holes) that extend entirely through layer 18 to an underlying layer, and is preferably deposited to a thickness of at least about 600Å. However, in some embodiments holes extending entirely through layer 18 will be of little or no consequence in semiconductor circuitry ultimately formed from layer 18. Such embodiments can include, for example, embodiments wherein adhesion layer 16 is provided beneath platinum-comprising layer 18. Accordingly, in embodiments wherein platinum layer 18 is provided over an adhesion layer 16, it can be preferred to provide platinum layer 18 to a thickness of less than 400Å because of space limitations due to the close packing of capacitors. Also, in embodiments in which platinum layer 18 is utilized in forming circuitry having tight spacing requirements it can be preferred to form layer 18 to be

relatively thin. For instance, in some capacitor constructions it can be desired to form layer 18 to be less than or equal to about 1000Å, and more preferred to form layer 18 to be from about 300Å to about 400Å to avoid electrical contact between adjacent capacitor structures.

A fragmentary top view of wafer fragment 10 is shown in Fig. 2. Layer 18 is preferably a continuous layer (defined as a layer without cavities extending therethrough to an underlying layer -- such as the underlying layer 16 of Fig. 2) across its entirety. Alternatively, some portion of layer 18 is continuous. For example, consider an application where layer 18 overlies and contacts a conductive layer to form a circuit device comprising both layer 18 and the underlying conductive layer. In such applications, it is generally still desired that a substantial portion of layer 18 be continuous to, for example, maintain a uniform electrical contact between layer 18 and the underlying conductive layer. Such substantial portion will preferably cover a surface area of at least about 4×10^6 square Angstroms. A surface area of about 4×10^6 square Angstroms is illustrated in Fig. 3 as a square 50 having sides of about 2000 Angstroms.

Fig. 3 illustrates an embodiment wherein platinum-comprising layer 18 is incorporated into a capacitor construction 30 as a storage node. Specifically, a dielectric layer 22 and a capacitor electrode 24 are provided over platinum-comprising layer 18 to form capacitor construction 30. Dielectric layer 22 can comprise one or more of silicon

oxide or silicon nitride, or it can comprise other dielectric materials, such as, for example, tantalum pentoxide, or $BaSrTiO_3$. Capacitor electrode 24 can comprise, for example, TiN, conductively doped silicon (such as polysilicon), or a metal, such as, for example, platinum. In embodiments wherein capacitor electrode 24 comprises platinum, capacitor electrode 24 can be formed by chemical vapor deposition over dielectric layer 22. The chemical vapor deposition can be conducted either to form upper electrode 24 with a relatively smooth upper surface, or to form upper electrode 24 with a relatively rough upper surface. If capacitor electrode 24 is to be formed of platinum with a relatively smooth upper surface, it can be chemical vapor deposited in a reaction chamber with a temperature maintained at above about 300° C and/or with an oxidizing gas flow rate of less than 50 sccm and a carrier gas flow rate of greater than 30 sccm. Also, any platinum comprised by capacitor electrode 24 can be in the form of elemental platinum, or an alloy, such as, for example, rhodium/platinum alloy.

As shown, layer 18 has a rough outer surface and layers 22 and 24 are conformal to the rough outer surface of layer 18.

Figs. 4 and 5 illustrate scanning electron microscope (SEM) micrographs of platinum films produced by CVD of $MeCpPt(Me)_3$. Fig. 4 illustrates a surface produced within a reaction chamber in a time of about 6 minutes, wherein a temperature in the chamber was about 215°C, a pressure was about 5 Torr, a flow rate of carrier gas

(He, with a pressure at the carrier gas bubbler of about 6 Torr) was about 5 sccm, and a flow rate of oxidizing gas (O_2) was about 50 sccm. The platinum surface formed comprises pedestals characteristic of columnar growth. The columnar pedestals terminate in dome-shaped (substantially hemispherical) tops. It can be advantageous to have substantially hemispherical tops, rather than tops having sharp edges, in forming capacitor constructions or other electronic circuitry from a deposited platinum layer. Specifically, the relatively rounded hemispherical surfaces can create relatively uniform electric fields at the surface of a deposited platinum layer. In contrast, if sharp edges were present, the sharp edges could form loci for high electric fields, and lead to leakage of electric current across the capacitor. The platinum layer illustrated in Fig. 4 can be referred to as "hemispherical grain" platinum to indicate a structure largely analogous to a material known in the art as hemispherical grain polysilicon.

The platinum layer of Fig. 4 is characterized by columnar pedestals generally having heights greater than or equal to about one-third of a total thickness of the platinum layer. Many of the pedestals shown in Fig. 4 have a height approximately equal to a thickness of the deposited platinum layer. Accordingly, if the deposited platinum layer has a thickness of about 600Å, the individual pedestals can have a thickness approaching 600Å. Such is only an approximation to the size of the pedestals as it is found that some of the pedestals will grow from

surfaces of other pedestals, and some of the pedestals will grow less vertically than other pedestals. An average diameter of the pedestals is about 200Å, and the pedestals are generally closely packed (i.e., the pedestals generally touch other pedestals and many pedestals fuse with other pedestals), but the distribution of the pedestals is typically not a close-packed structure (i.e., a structure wherein all the pedestals are tightly packed in, for example, an hexagonal type arrangement to form a maximum number of pedestals on a given surface). The columnar growth illustrated in Fig. 4 is found not to occur if a temperature within a CVD reaction chamber is above 300°C.

Fig. 5 illustrates a surface produced on a platinum film within a reaction chamber in a time of about 150 seconds, wherein a temperature in the chamber was 300°C, a pressure was about 0.5 Torr, a flow rate of carrier gas (He, with a pressure at the carrier gas bubbler of about 6 Torr) was about 30 sccm, and a flow rate of oxidizing gas (O_2) was about 10 sccm. The platinum layer deposited under the Fig. 5 conditions has a much smoother surface than that deposited under the Fig. 4 conditions. Figs 4 and 5 together evidence that it is possible to control a grain structure of a surface of a chemical vapor deposited platinum layer by controlling process parameters of a chemical vapor deposition reaction chamber.

Although the invention has been described with application to formation of a capacitor structure, it is to be understood that the

invention can be utilized in a number of other applications as well. For instance, a platinum layer having a roughened surface can be utilized for formation of catalysts.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A method of forming a roughened layer of platinum, comprising:

providing a substrate within a reaction chamber;

flowing an oxidizing gas into the reaction chamber;

flowing a platinum precursor into the reaction chamber and depositing platinum from the platinum precursor over the substrate in the presence of the oxidizing gas; and

maintaining a temperature within the reaction chamber at from about 0°C to less than 300°C during the depositing.

2. The method of claim 1 further comprising providing a reactant in contact with the roughened layer of platinum and utilizing the platinum to catalyze a conversion of the reactant to a product.

3. The method of claim 1 wherein the flowing the platinum precursor comprises flowing a carrier gas carrying the platinum precursor, the carrier gas being flowed at a rate of no greater than about 30 sccm and the oxidizing gas being flowed at a rate of at least about 50 sccm.

4. The method of claim 1 wherein the oxidizing gas comprises at least one of O_2, N_2O, SO_3, O_3, H_2O_2, or NO_x, wherein x has a value of from 1 to 3.

5. The method of claim 1 wherein the platinum precursor comprises at least one of $MeCpPtMe_3$, $CpPtMe_3$, $Pt(acetylacetonate)_2$, $Pt(PF_3)_4$, $Pt(CO)_2Cl_2$, cis-$[PtMe_2(MeNC)_2]$, or platinum hexafluoroacetylacetonate.

6. The method of claim 1 wherein the maintaining comprises maintaining the temperature at from about 200°C to less than 300°C.

7. The method of claim 1 wherein the maintaining comprises maintaining the temperature at from about 220°C to about 280°C.

8. The method of claim 1 further comprising forming an adhesion layer over the substrate and depositing the platinum onto the adhesion layer.

9. The method of claim 8 wherein the adhesion layer comprises at least one of titanium nitride, iridium, rhodium, ruthenium, platinum, palladium, osmium, silver, rhodium/platinum alloy, IrO_2, RuO_2, RhO_2, or OsO_2.

10. The method of claim 1 further comprising flowing at least one other metal precursor into the chamber in addition to the platinum precursor, and wherein the platinum is deposited as an alloy of platinum and the at least one other metal.

11. The method of claim 1 further comprising flowing a second metal precursor into the chamber and wherein the platinum is deposited as an alloy of platinum and the second metal.

12. The method of claim 11 wherein the second metal is rhodium, iridium, ruthenium, palladium, osmium, or silver.

13. The method of claim 1 wherein the platinum is deposited to a thickness of at least about 400Å.

14. The method of claim 1 wherein the maintaining comprises maintaining the temperature at from about 200°C to less than 300°C, and wherein the platinum is deposited to a thickness of at least about 600Å in a time of less than about 40 seconds.

15. A method of forming a roughened layer of platinum, comprising:

providing a substrate within a reaction chamber;

flowing an oxidizing gas into the reaction chamber;

flowing a platinum precursor into the chamber and depositing platinum from the platinum precursor over the substrate in the presence of the oxidizing gas;

maintaining a temperature within the chamber at from about 0°C to less than or equal to about 280°C during the depositing, the deposited platinum having a rougher surface than it would have if the temperature were 300°C or greater during the depositing.

16. The method of claim 15 wherein the deposited platinum forms a continuous layer over a surface area that is at least 4 x 10^6 square Angstroms.

17. The method of claim 15 wherein the deposited platinum is hemispherical grain platinum.

18. A method of forming a capacitor, comprising:

providing a substrate within a reaction chamber;

flowing a first oxidizing gas into the reaction chamber;

flowing a first platinum precursor into the chamber and depositing platinum from the first platinum precursor over the substrate in the presence of the first oxidizing gas while maintaining a temperature within the chamber at from about 0°C to less than 300°C, and providing the deposited platinum into a first capacitor electrode;

forming a second capacitor electrode proximate the first capacitor electrode; and

forming a dielectric layer proximate the first capacitor electrode, the dielectric layer being between the first and second capacitor electrodes.

19. The method of claim 18 wherein the flowing the first platinum precursor comprises flowing a carrier gas carrying the platinum precursor, the carrier gas being flowed at a rate no greater than 30 sccm and the first oxidizing gas being flowed at a rate of at least 50 sccm.

20. The method of claim 18 wherein the forming the second capacitor electrode comprises depositing platinum from a second platinum precursor in the presence of a second oxidizing gas.

21. The method of claim 20 wherein the second platinum precursor is the same as the first platinum precursor.

22. The method of claim 20 wherein the second oxidizing gas is the same as the first oxidizing gas.

23. The method of claim 20 further comprising flowing a second metal precursor into the chamber with the first platinum precursor, and wherein the platinum is deposited as an alloy of platinum and the second metal.

24. The method of claim 23 wherein the second metal is rhodium, iridium, ruthenium, palladium, osmium, or silver.

25. The method of claim 18 further comprising forming an adhesion layer over the substrate and depositing the platinum onto the adhesion layer.

26. The method of claim 25 wherein the adhesion layer comprises at least one of titanium nitride, iridium, rhodium, ruthenium, platinum, palladium, osmium, silver, rhodium/platinum alloy, IrO_2, RuO_2, RhO_2, or OsO_2.

27. The method of claim 18 wherein the maintaining comprises maintaining the temperature at from about 200°C to less than 300°C.

28. The method of claim 18 wherein the maintaining comprises maintaining the temperature at from about 220°C to about 280°C.

29. A circuit comprising:

a semiconductive substrate; and

a roughened platinum layer over the substrate, the roughened platinum layer comprising hemispherical grain platinum.

30. A circuit comprising:

a semiconductive substrate; and

a roughened platinum layer over the substrate, the roughened platinum layer being continuous over an area of the substrate that comprises at least about 4 x 10^6 square Angstroms and comprising pedestals that are at least about 300Å tall within the area.

31. The circuit of claim 30 wherein the platinum layer comprises hemispherical grain platinum.

32. The circuit of claim 30 wherein the area of the substrate comprises a square.

33. A circuit comprising:

a semiconductive substrate; and

a roughened platinum layer over the substrate, the roughened platinum layer having a continuous surface characterized by columnar pedestals having heights greater than or equal to about one-third of a total thickness of the platinum layer.

34. The circuit of claim 33 wherein the platinum layer has a thickness of at least about 600Å.

35. The circuit of claim 33 wherein the platinum layer has a thickness of greater than or equal to about 400Å.

36. The circuit of claim 33 wherein the platinum layer has a thickness of greater than or equal to about 100Å.

37. The circuit of claim 33 further comprising an adhesion layer between the platinum layer and the substrate, the adhesion layer comprising at least one of titanium nitride, iridium, rhodium, ruthenium, platinum, palladium, osmium, silver, rhodium/platinum alloy, IrO_2, RuO_2, RhO_2, or OsO_2.

38. The circuit of claim 33 wherein the pedestals terminate in dome-shaped tops.

39. The circuit of claim 33 wherein the pedestals terminate in hemispherical tops.

40. A capacitor comprising:

a first capacitor electrode;

a second capacitor electrode;

a dielectric layer between the first and second capacitor electrodes; and

wherein at least one of the first and second capacitor electrodes comprises a roughened platinum layer, the roughened platinum layer having a thickness of from about 400Å to about 1000Å and comprising pedestals that are at least about 300Å tall.

41. The capacitor of claim 40 wherein the roughened platinum layer comprises hemispherical grain platinum.

42. The capacitor of claim 40 wherein the roughened platinum layer is over a surface and is continuous over an area of the surface that is at least about 4 x 10^6 square Angstroms.

43. The capacitor of claim 42 wherein the area comprises a square.

44. A capacitor comprising:

a first capacitor electrode;

a second capacitor electrode;

a dielectric layer between the first and second capacitor electrodes; and

wherein at least one of the first and second capacitor electrodes comprises a roughened platinum layer, the roughened platinum layer having a continuous surface characterized by columnar pedestals having heights greater than or equal to about one-third of a total thickness of the platinum layer.

45. The capacitor of claim 44 wherein both capacitor electrodes comprise platinum, but only one of the capacitor electrodes comprises the roughened platinum layer.

46. The capacitor of claim 44 wherein both capacitor electrodes comprise roughened platinum layers.

47. The circuit of claim 44 wherein the pedestals terminate in dome-shaped tops.

48. The circuit of claim 44 wherein the pedestals terminate in hemispherical tops.

49. A platinum-containing material, comprising:

a substrate; and

a roughened platinum layer over the substrate, the roughened platinum layer having a continuous surface characterized by columnar pedestals having heights greater than or equal to about one-third of a total thickness of the platinum layer.

50. The material of claim 49 wherein the pedestals terminate in dome-shaped tops.

51. The material of claim 49 wherein the pedestals terminate in hemispherical tops.

52. A reaction catalyst comprising hemispherical grain platinum.

53. A reaction catalyst characterized by an outer surface portion of platinum comprising a plurality of columnar pedestals that are at least about 100Å tall.

54. The catalyst of claim 53 wherein the columnar pedestals are at least about 400Å tall.

55. The catalyst of claim 53 wherein the platinum comprises hemispherical grain platinum.

56. The catalyst of claim 53 wherein the surface portion is continuous over a substrate and covers an area of the substrate that is at least about 4×10^6 square Angstroms.

ABSTRACT OF THE DISCLOSURE

In one aspect, the invention includes a method of forming a roughened layer of platinum, comprising: a) providing a substrate within a reaction chamber; b) flowing an oxidizing gas into the reaction chamber; c) flowing a platinum precursor into the reaction chamber and depositing platinum from the platinum precursor over the substrate in the presence of the oxidizing gas; and d) maintaining a temperature within the reaction chamber at from about 0°C to less than 300°C during the depositing. In another aspect, the invention includes a platinum-containing material, comprising: a) a substrate; and b) a roughened platinum layer over the substrate, the roughened platinum layer having a continuous surface characterized by columnar pedestals having heights greater than or equal to about one-third of a total thickness of the platinum layer.

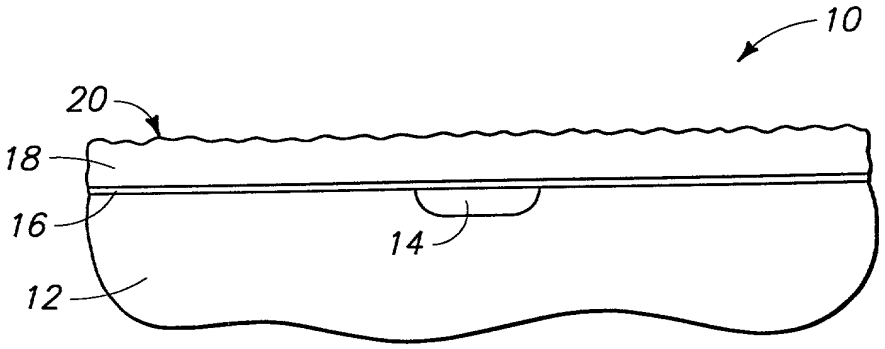


Fig 1

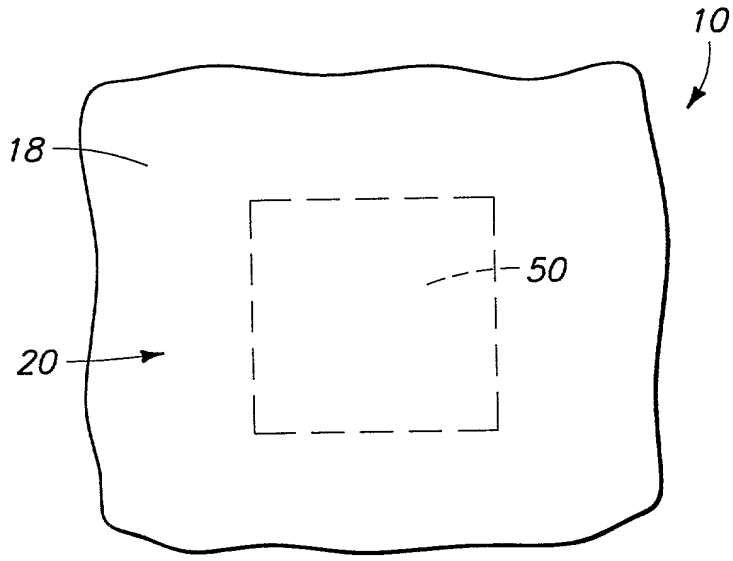


Fig 2

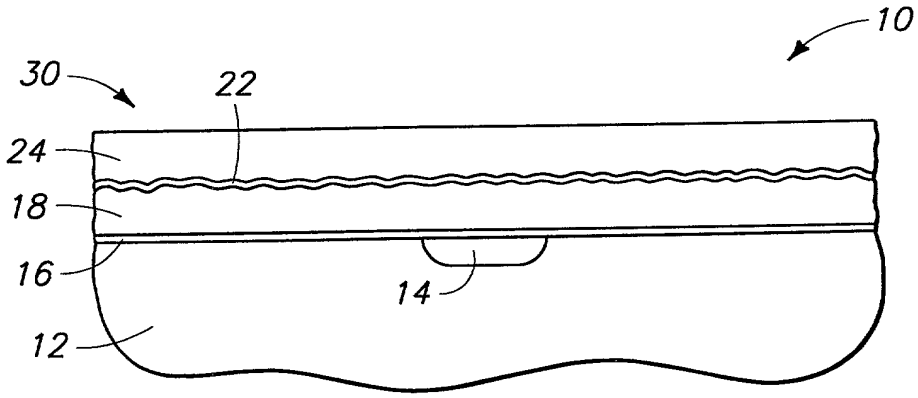
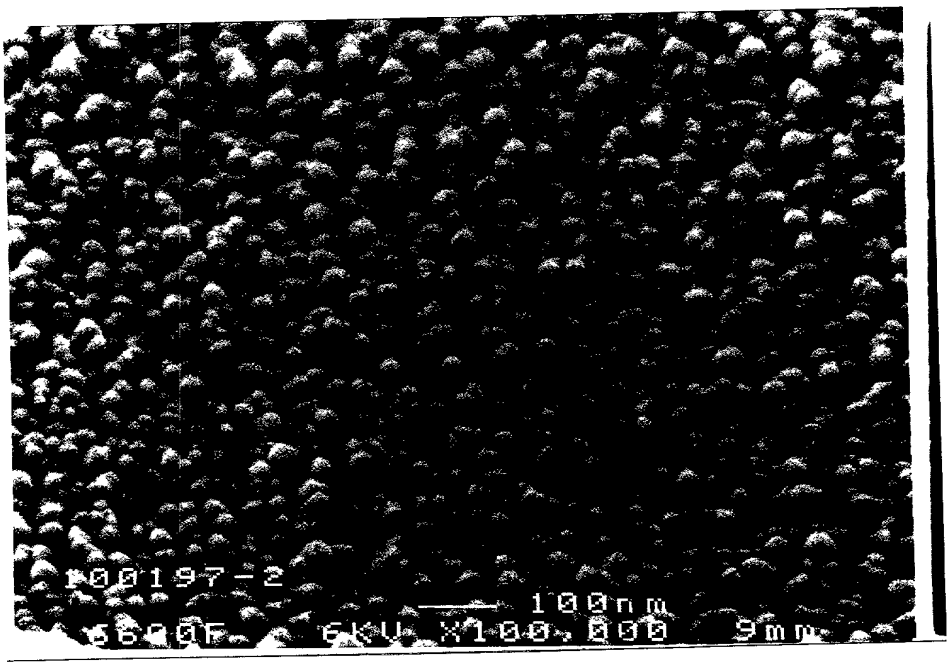
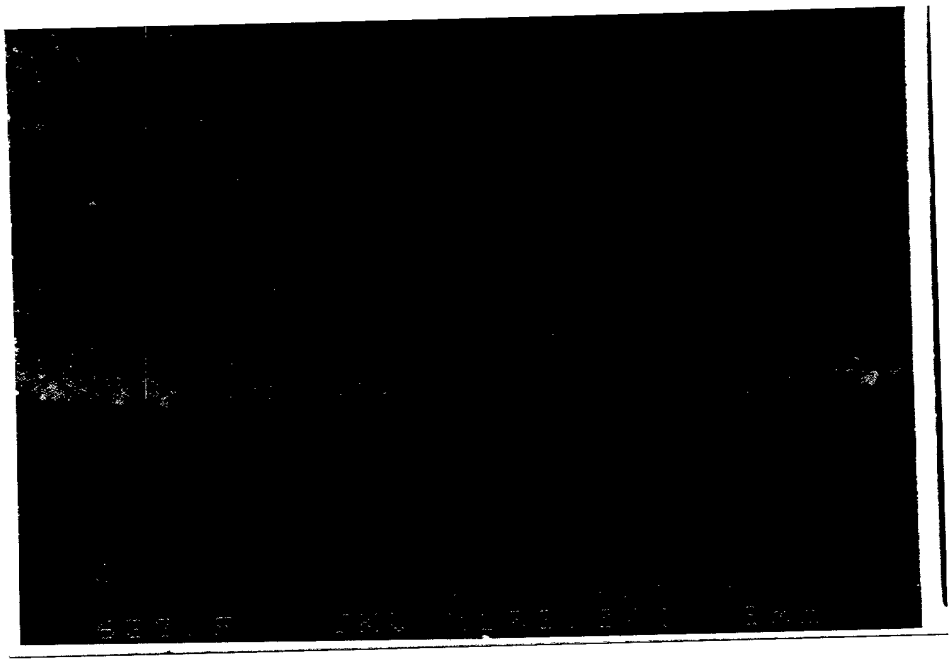


Fig 3



Фиг 4



Фиг 5

Addendum

1. Circuitry Comprising Roughened Platinum Layers, Platinum-Containing Materials, Capacitors Comprising Roughened Platinum Layers, Methods of Forming Roughened Layers of Platinum, and Methods of Forming Capacitors
2. - Petition to Accept Photograph(s) as Drawing(s)
   - 1 set of photographs

DECLARATION OF SOLE INVENTOR FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Circuitry Comprising Roughened Platinum Layers, Platinum-Containing Materials, Capacitors Comprising Roughened Platinum Layers, Methods Of Forming Roughened Layers Of Platinum, And Methods Of Forming Capacitors, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so

made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * * *

Full name of sole inventor: **Eugene P. Marsh**

Inventor's Signature: Eugene P Marsh

Date: 8/24/98

Residence: **Boise, Idaho**

Citizenship: **U.S.**

Post Office Address: **1722 Picabo Ct., Boise, ID 83716**